Claims

What is claimed is:

1. A random access memory (RAM) circuit coupled to a write control line, a read control line, and at least one bitline, the RAM circuit comprising:

a write switch having a control terminal and first and second terminals, the first terminal of the write switch coupled to the at least one bitline, the control terminal of the write switch coupled to the write control line;

a charge-storage device having first and second terminals, wherein the first terminal of the charge-storage device is coupled to the second terminal of the write switch and the second terminal of the charge-storage device is coupled to the read control line; and

a read switch having a control terminal and first and second terminals, the control terminal of the read switch coupled to the first terminal of the charge-storage device and coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the at least one bitline, and the second terminal of the read switch coupled to ground.

2. The RAM circuit of claim 1, wherein the charge-storage device is a capacitor.

3. The RAM circuit of claim 1, wherein the at least one bitline comprises a write bitline and a read bitline, the first terminal of the write switch is coupled to the write bitline, and the first terminal of the read switch is coupled to the read bitline.

4. The RAM circuit of claim 1, wherein the write switch is a write transistor, the read switch is a read transistor, the control terminal for each of the write and read transistors is a gate terminal, and the first and second terminals for each of the write and read transistors are source/drain terminals.

5. The RAM circuit of claim 4, wherein the read transistor has a threshold voltage and the threshold voltage, during a read operation when a predetermined voltage is placed on the read control line, is between a cell voltage used to store a first data value and a cell voltage used to store a second data value.

6. The RAM circuit of claim 5, wherein the threshold voltage of the read transistor is between about 0.6 volts and about 1.2 volts.

7. The RAM circuit of claim 5, wherein the first data value corresponds to a zero and the second data value corresponds to a one.

8. The RAM circuit of claim 1, wherein the first terminal of the read switch is coupled to the at least one bitline solely through one or more conductive connections.

9. A method of using a random access memory (RAM) circuit, the RAM circuit coupled to a write control line, a read control line and at least one bitline, the method comprising the steps of:

placing a predetermined bitline voltage on the at least one bitline, the predetermined voltage corresponding to a value to be stored in the RAM circuit;

placing a predetermined write control voltage on the write control line, the write control line coupled to a control terminal of a write switch, the write switch further comprising first and second terminals, the first terminal of the write switch coupled to the at least one bitline, the control terminal of the write switch coupled to the write control line;

placing a predetermined low voltage on the read control line, the read control line coupled to a second terminal of a charge-storage device, the charge-storage device further comprising a first terminal, wherein the first terminal of the charge-storage device is coupled to the second terminal of the write switch; and placing a predetermined high voltage on the read control line.

10. The method of claim 9, further comprising the step of maintaining the predetermined low voltage for a predetermined time period.

11. The method of claim 10, wherein the predetermined time period ends before the voltage that turns off the write switch is placed on the write control line, whereby there is a stored voltage at the first terminal of the charge storage device.

12. The method of claim 11, wherein the predetermined low voltage is negative and the predetermined high voltage is a ground voltage.

13. The method of claim 11, wherein the predetermine low voltage is ground voltage and the predetermined high voltage is above ground voltage.

14. The method of claim 11, wherein the predetermined bitline voltage is a voltage corresponding to a data one, wherein the predetermined write control voltage and predetermined bitline voltage are selected so that the write switch is turned off when the predetermined write control voltage is placed on the write control line, the predetermined bitline voltage is placed on the at least one bitline, and the predetermined high voltage is placed on the read control line, whereby the stored voltage may be higher than the predetermined bitline voltage.

15. The method of claim 11, wherein the predetermined bitline voltage is a voltage corresponding to a data zero, wherein the predetermined write control voltage and predetermined bitline voltage are selected so that the write switch is turned on when the predetermined write control voltage is placed on the write control line, the predetermined bitline voltage is placed on the at least one bitline, and the predetermined high voltage is

placed on the read control line, whereby the stored voltage may be the same as the predetermined bitline voltage.

16. The method of claim 11, and wherein the first terminal of the charge-storage device is further coupled to a control terminal of a read switch, the read switch further having first and second terminals, the control terminal of the read switch also coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the at least one bitline, and the second terminal of the read switch coupled to ground.

17. The method of claim 16, further comprising the steps of:

placing a second predetermined bitline voltage on the at least one bitline;

placing a read voltage on the read control line, the read voltage selected so that the read switch is turned on;

sensing voltage on the at least one bitline; and

using the sensed voltage to determine a value corresponding to the sensed voltage.

18. The method of claim 17, wherein the second predetermined bitline voltage is between about 0.4 volts to about 1.0 volts.

19. A semiconductor memory device comprising:

a read transistor comprising first and second source/drain areas formed on sides of a first diffusion area, a gate formed above the first diffusion area, and a gate insulator positioned between the gate and the first diffusion area;

a conductive layer, the conductive layer and the gate of the read transistor at least partially overlapping;

an insulator formed between the gate of the read transistor and the conductive layer, wherein the conductive layer, gate of the read transistor, and insulator form a charge-storage device;

a write transistor comprising first and second source/drain areas formed on sides of a second diffusion area, a gate formed above the second diffusion area, and a gate insulator positioned between the gate and the second diffusion area; and

a coupling device that couples the first source/drain area of the write transistor to the charge storage device.

20. The semiconductor memory device of claim 19, wherein the first and second diffusion areas are a single diffusion area.

21. The semiconductor memory device of claim 19, further comprising at least one bitline coupled to the first source/drain area of the read transistor and to the second source/drain area of the write transistor.

22. The semiconductor memory device of claim 19, wherein the charge-storage device is a capacitor, and wherein the coupling device couples the first source/drain area of the write transistor to the gate of the read transistor.

23. The semiconductor memory device of claim 22, wherein the conductive layer abuts the insulator and the insulator abuts the gate of the read transistor.

24. The semiconductor memory device of claim 23, wherein the conductive layer comprises n+ doped polysilicon and the gate of the read transistor comprises p+ doped polysilicon.

25. The semiconductor memory device of claim 24, wherein the coupling device comprises a metal layer at least partially overlying both the first source/drain area of the write transistor and the gate of the read transistor.

26. The semiconductor memory device of claim 24, wherein the coupling device comprises a metal layer coupled to a first connection that contacts the first source/drain area of the write transistor, the metal layer further coupled to a second connection that contacts the gate of the read transistor.

27. The semiconductor memory device of claim 23, wherein the conductive layer comprises a metal layer and the gate of the read transistor comprises tungsten.

28. The semiconductor memory device of claim 27, wherein the coupling device comprises a metal layer coupled to a first connection that contacts the first source/drain area of the write transistor, and the metal layer is further coupled to a second connection that contacts the gate of the read transistor.

29. The semiconductor memory device of claim 27, wherein a portion of the gate of the read transistor overlies the first source/drain area of the write transistor and wherein the coupling device comprises a tungsten layer formed integrally with the gate of the read transistor and formed between the portion of the gate of the read transistor and the first source/drain area of the write transistor.

30. An integrated circuit device comprising at least one bitline, a ground, and at least one random access memory circuit, the at least one memory circuit comprising:

at least one semiconductor memory device comprising:

a read transistor comprising first and second source/drain areas formed on sides of a first diffusion area, a gate formed above the first diffusion area, and a gate insulator positioned between the gate and the first diffusion area, the first source/drain area of the read transistor is coupled to the at least one bitline, and wherein the second source/drain area of the read transistor is coupled to the ground;

a conductive layer, the conductive layer and the gate of the read transistor at least partially overlapping;

an insulator formed between the gate of the read transistor and the conductive layer, wherein the conductive layer, gate of the read transistor, and insulator form a charge-storage device;

a write transistor comprising first and second source/drain areas formed on sides of a second diffusion area, a gate formed above the second diffusion area, and a gate insulator positioned between the gate and the second diffusion area, wherein the second source/drain area of the write device is coupled to the at least one bitline; and

a coupling device that couples the first source/drain area of the write transistor to the charge storage device.

31. A semiconductor memory device comprising:

a read transistor comprising first and second source/drain areas formed on sides of a first diffusion area, a gate formed above the first diffusion area, and a gate insulator positioned between the gate and the first diffusion area, wherein a channel region is formed in the first diffusion area underneath the gate and between the first and second source/drain areas;

a write transistor comprising first and second source/drain areas formed on sides of a second diffusion area, a gate formed above the second diffusion area, and a gate insulator positioned between the gate and the second diffusion area;

a conductive layer, the conductive layer and the channel region of the read transistor at least partially overlapping;

an insulator formed between the first diffusion area and the conductive layer and formed abutting a bottom of the first diffusion area and abutting a surface of the conductive layer; and

a coupling device that couples the first source/drain area of the write transistor to the conductive layer.

32. The semiconductor memory device of claim 31, wherein the coupling device is formed integrally with the conductive layer.

33. The semiconductor memory device of claim 31, wherein the conductive layer comprises polysilicon.

34. The semiconductor memory device of claim 31, wherein a trench isolation is formed between the second source/drain area of the read transistor and the first source/drain area of the write transistor.

35. The semiconductor memory device of claim 31, wherein the conductive layer is formed in an insulating layer.

36. A method for using a memory device coupled to at least one bitline, a write control line and a read control line, the method comprising the steps of:

placing one of two predetermined voltages on the at least one bitline while also placing a first predetermined write voltage on the write control line, the memory device comprising:

a read transistor comprising first and second source/drain areas formed on sides of a first diffusion area, a gate formed above the first diffusion area, and a gate insulator positioned between the gate and the first diffusion area, wherein the first source/drain area of the read transistor is coupled to the at least one bitline and the gate of the read transistor is coupled to the read control line, and wherein a channel region is formed in the first diffusion area underneath the gate and between the first and second source/drain areas;

a write transistor comprising first and second source/drain areas formed on sides of a second diffusion area, a gate formed above the second diffusion area, and a gate insulator positioned between the gate and the second diffusion area, wherein the second source/drain area of the write transistor is coupled to the at least one bitline and the gate of the write transistor is coupled to the write control line;

the conductive layer, wherein the conductive layer and the channel region of the read transistor at least partially overlaps;

an insulator formed abutting a bottom of the first diffusion area and abutting a surface of the conductive layer; and

a coupling device that couples the first source/drain area of the write transistor to the conductive layer,

wherein the first predetermined write voltage is suitable to enable the write transistor; and

placing a second predetermined write voltage on the write control line, the second predetermined write voltage suitable to disable the write transistor.

37. The method of claim 36, wherein the two predetermined voltages each corresponds to a predetermined value, and wherein the method further comprises the steps of:

placing a predetermined bitline voltage on the at least one bitline;

placing a first predetermined read voltage on the read control line, the first predetermined read voltage suitable for enabling the read transistor; and

sensing fluctuations, if any, on the at least one bitline to determine which of the two predetermined values is stored in the memory device.

38. The method of claim 37, wherein the fluctuations are one or more of voltage fluctuations and current fluctuations.